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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SHINGLETON, MICHAEL B	
ART UNIT	**PAPER NUMBER**
2817	

DATE MAILED: 07/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/646,936	NAFFZIGER ET AL.	
	Examiner	Art Unit	
	Michael B. Shingleton	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-11,14-27 and 30-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-7, 10, 11, 14, 16, 17, 19-27 and 30-32* is/are rejected.

7)☒ Claim(s) *8,9,15 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Michael B. Shingleton

MICHAEL B SHINGLETON
PRIMARY EXAMINER
ART UNIT 2817

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 10, 11, 14, 16, 23-27, and 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lipton 5,181,133 (Lipton) in view of Horn "Basic Electronics" (Horn).

Figures 4, 5 and 5a as well as the relevant text of Lipton disclose a system or device that includes the production of a "temporarily modified output". The device of Lipton produces the waveforms shown in Figures 4, 5 and 5a that shows a waveform that transitions directly between high and low levels in a periodical fashion (Note Figure 5 and the first part (left-hand side) of Figure 5a.). This is what applicant refers to in some of the claims as "a second operating mode". Lipton does operate in this second operating mode for the open state. The "first operating mode" as called by some of the claims of the instant invention relates to the waveform where the signal transitions directly from the high level to an intermediate level and then directly transitions from this intermediate level to the low level and then transitions directly from this low level back to the intermediate level. This is clearly shown in Figure 4 and the second half (right-hand side) of Figure 5a of Lipton. Lipton is silent on the details of the structure that makes up this device sometimes called a "waveform control" in some of the claims. Lipton is also silent on the use of a driver to provide the final output signal.

Even though Lipton is silent on the specific structure that makes up the "waveform control", there must be something in this structure of Lipton that sets forth the time period for the time the waveform is to remain at the intermediate level. Thus this structure can therefore be called "delay network" as this "delay network" provides a control or the setting of the time period that waveform is to remain at the intermediate level. In other words it delay the application of the next high or low level by a certain predetermined delay and thus is s delay network. In addition it is noted that applicant does not specifically define exactly what a "delay network" is to mean. For example applicant has not defined "delay network" as meaning only a length of micro-strip delay line of one meter in length. Thus given the

broadest reasonable interpretation and the plain meaning of the terminology, any structure that determines or sets a delay is a delay network. This is only reasonable. Additionally a different reading of the claims would also allow for this circuitry to be called a delay network, since the circuitry that sets the time period for the intermediate level is composed of real world elements in Lipton and real world elements have delay.

Lipton does lack the showing of a driver or buffer that outputs the final signal form the so called "waveform control". However, the use of buffers as the final driver for a circuit is well known in the circuitry art so as to allow for sufficient output drive and to allow for multiple loads to be driven if desired. See page 377 and 378 of Horn.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided a buffer a the output of the circuit that provides the waveforms as indicated and shown in Figures 4, 5 and 5a of Lipton so as to for sufficient drive as taught by Horn.

With respect to independent claim 14 and any of those claims dependent thereon that is part of this rejection all the reasoning above and the following: Applicant calls the device a "clock" which Lipton is silent on the naming the device a "clock", applicant also states that a "predriver coupled to control the waveform control" is present (Note that the "waveform control" is the structure that produces the two modes of operation or the two waveforms indicated above.), applicant further states that "a least one associated circuit is driven by the output clock" and applicant further states that "the at least one associated circuits further comprising a precharge device that provides a charge at an associated node based on the output clock signal". Note that the circuitry of Lipton is to be an integrated circuit as clearly shown in Figure 2. The naming of the device a "clock" is merely a statement of intended use. Any square wave or stair step waveform generator can be considered to be a "clock" for it generates a signal that is referenced to time i.e. it has a predetermined period. In order to explain this to applicant, lets say that the structure of a function generator is provided wherein that waveform function generator provides either a square wave or a stair step waveform and the claim in a patent application is directed to structure. MPEP 2114 states that claims directed to structure must be distinguished by structure. The fact that the waveform generator can be used as a "clock" in a digital system does not change the structure of the waveform generator. It is merely explains one use the claimed structure is capable of performing. The same goes with the waveform generator disclosed in Lipton. Even though Lipton's preferred use is to drive a liquid crystal shutter this does not mean that the waveform generator structure therein cannot be used elsewhere or is not capable of being used elsewhere. Accordingly, as Lipton is fully capable of performing as a clock, it meets the claim limitation of being capable of being a clock (See MPEP 2114

and In re Schreiber, 128 F.3d 1473, 1477-78, 44USPQ2d 1429, 1431-32 (Fed. Cir. 1997). No structural difference is recited by the limitation of being a "clock". There is also a structure in Lipton that tells the device of Lipton to switch from an open shutter to one that is the in the "shuttering state", this would be the claimed "predriver coupled to control the waveform control" in Lipton. Something has to tell the waveform generator of Lipton to now switch from providing an open state to a shuttering state. The claimed "associated circuit" would be the load or the shutter in Lipton. The shutter is a "precharge device that provides a charge at an associated node based on the clock signal" for a liquid crystal is a capacitance device that stores charge. The above is just reading the claims with the broadest reasonable interpretation consistent with the specification See MPEP 2111. Furthermore since applicant has not provided any specific definitions for these terms used in the claims the examiner has only given the plain meanings to these terms (See MPEP 2111.01). Also note that this reasoning concerning the "precharge device" being the shutter is the means for supplying a charge to a node of "associated circuitry" wherein this charge is a supplemental charge. This supplement charge would be "commensurate with a duration that the clock signal is provided at the intermediate level (Emphasis added)". Note that the reasoning presented in the rejection of claim 27 below applies here for the last section of claim 31 where the functional language recites evaluation of circuitry without there being any evaluation circuitry claimed. This is merely setting forth an intended use and not further distinguishing structure and since the waveform generator of the prior art produces the same waveforms of the disclosed waveform generator the waveform generator of the prior art is fully capable of performing the recited intended use. Also "a duration" could be the entire duration of the intermediate level or any part of the duration at the intermediate level.

With respect to independent claim 16 note all the reasoning above.

With respect to independent claim 30 and any dependent claim thereon indicated as rejected above as well as claim 23 note all the reasoning above and the following: Applicant has not made a positive statement that applicant has invoked 35 USC 112 sixth paragraph. However, the examiner's position is that the devices, i.e. means, indicted above will provide the means or equivalents thereto as recited by claim 30 and any dependent claim indicted in the claims rejected above. In the device of Lipton, the intermediate level would be a level "that self-biases between normal high and low levels according to process variations in the system" or the "self-biases to...during the second operating mode based on relative characteristics of at least some components that form the driver". What applicant recites in the specification is that normal device tolerances will determine the exact biasing point or intermediate level point. Such is the case with Lipton for example how large the capacitance is of the liquid crystal shutter is one structure that helps determine what the intermediate level will be and the capacitance of the

device is "depended on process variations" as recited by the specification. Furthermore the driver characteristics like the "at rest" current etc. helps determine what the intermediate level will be.

With respect to dependent claim 10 and the last part of claim 25 (The subject matter of the first part of claim 25 is clearly addressed above and accordingly does not need to be repeated here.), the capacitance of the liquid crystal as noted above acts as a precharge device that charges, i.e. partially conducts to, an associated node based on the output signal provided by the driver. During charging/discharging the capacitance or precharge device partially conducts based on the intermediate level of the output signal during the first operating mode. Note that discharging to a node is charging that node. Thus since the condition that defines the function of "thereby operating as a supplemental keeper to precharge the associated node" is clearly provided for, i.e. the precharge device charges an associated node based on the output signal provided by the driver, the function of "thereby operating as a supplemental keeper to precharge the associated node" is clearly provided for. Note that no specific definition of exactly what is to compose a "supplemental keeper" is provided for in the original disclosure. Claim 11 contains the same subject matter as that of the last part of claim 30 already addressed above and thus applicant is referred to that discussion above. With respect to claim 27 here the same subject matter of having a precharge device that partially conducts is recited. The functional language "whereby evaluation of the at least one circuit during the noise reduction mode is facilitated" is silent in the prior art. However, the claims do not recite any structure to enable this function either other than the structure of the precharge device that partially conducts. NO evaluation circuitry is recited and as such clearly the waveform generator like the waveform generator would be fully capable of performing the function and as no further distinguishing structure is recited by the claim this claim is seen as being anticipate by the prior art indicated above in accordance with MPEP 2114 and In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997).

Claims 3-7, 17, 19, 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lipton 5,181,133 (Lipton) in view of Horn "Basic Electronics" (Horn) as applied to claims above, and further in view of Patel et al. 5,296,756 (Patel)

Lipton and Horn are silent on the exact construction of the driver circuit.

One common form of art recognized equivalent driver circuit that provides stair-stepped waveform is the common inverter or push-pull structure where two transistors form a voltage divider across the supply voltage terminals. See transistors M1 and M2 of Patel and Figure 2 particularly the voltage at node "2".

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the driver of Lipton and Horn with one like Patel because as the Lipton and Horn references are silent on the exact structure of the driver one of ordinary skill in the art would have been motivated to use any art-recognized equivalent driver such as the driver taught by Patel. Note that the two terminals in the driver would have to be both at an intermediate level to provide the voltage dividing function to produce the intermediate level. (See claims 19, 21 and 22).

With respect to claim 6, see the above remarks concerning the last section of claim 30. With respect to claims 7 and 20, the above already address the two transistors of a first and second type.

With respect to claims 3 and 17, here applicant recites that the waveform control has one component that is coupled in such a way so as to "temporarily diode connect a transistor device of the driver to enable the driver to provide the output signal at the intermediate level for the duration of the first operating mode". The examiner has taken a broad interpretation of this term "diode connect" and applicant has objected in interviews between the examiner and applicant's representative. The examiner has gone to the specification and has found that the specification has and does support the examiner's broad interpretation of the term "diode connect" or "diode connection". Specifically, page 14 recites: "In one example implementation, NCKP at 216 is coupled to the gate of an output PFET. Thus, activation of M15 (e.g. in response to both NCKN and the feedback signal going low) results in a diode-connection of the output PFET. Accordingly, when M15 is activated during the noise reduction mode, the diode connection of the output PFET causes the clock signal CK to be provided at an intermediate level for a predetermined duration. Additionally, during the burn-in process, an NFET of the driver connected at 214 also is biased partially on such the burn-in condition, namely according to voltage at NCKN, such as can be provided by the associated predriver. (Emphasis added)". Thus with the low level being ground the transistor M1 of the driver like that in Patel must be biased at least partially on and thus form the temporarily diode connect as meant by applicant. With respect to claim 4 here applicant recites that the waveform control has a "logic network" that controls the operation of at least one component based on at least in part the delayed signal provided by the delay network. As stated above the device of Lipton has a delay network and this controls the circuit such that the various claimed waveforms are produced on "the at least one component" i.e. line. Since no specific definition is recited by applicant for "logic network" the circuitry of the "waveform control" of Lipton is seen as a "logic network" for it controls the switching of the output signal much like an "AND" gate or the like controls the switching of an output signal between different levels.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Figure 6 of Fawcett et al. 4,303,945 shows one conventional way to implement a waveform generator that switches between an intermediate level to a high level back to an intermediate level and then to a low level. Hedgecock 6,830,550 clearly shows that a generator that merely produces a waveform where the intermediate level is either between the high potential and the ground or is between the low potential and the ground just can not provide for a patentable distinction as this is known.

Claims 8, 9, 15, 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571) 272-1770.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306 and after .

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS
June 13, 2005

MICHAEL B SHINGLETON
PRIMARY EXAMINER
ART UNIT 2817